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IN THE CLAIMS

Claim 1 (Canceled).

Claim 2 (Original): A semiconductor package comprising:

a tape carrier;

a first semiconductor element having a surface and a first electrode, on which surface the first electrode is provided;

a longer lead having two ends and a first land, the one end being connected to the first electrode and the other end forming the first land on the tape carrier;

a second semiconductor element having a surface and a second electrode, on which surface the second electrode is provided, and the first semiconductor element is stacked;

a shorter lead having two ends and a second land, the one end being connected to the second electrode and the other end forming a second land on the tape carrier;

a resin material which seals the first semiconductor element, the second semiconductor element, the longer lead and the shorter lead; and

solder balls, which are mounted on the first and second lands for external connection.

Claim 3 (Canceled).

Claim 4 (Original). A semiconductor package according to claim 2, further comprising at least another longer lead and at least another shorter lead, wherein each of the longer leads and each of the shorter leads are arranged so as to alternate with each other.

Claim 5 (Canceled).

Claim 6 (Original): A semiconductor package according to claim 2, wherein the second semiconductor element is larger than the first semiconductor element, and comprises a surface area that faces the first semiconductor element and the second electrode is disposed outside said area.

Claim 7 (Canceled).

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Claim 8 (Original): A semiconductor package according to claim 2, wherein:
the first semiconductor element includes a first surface, on which the first electrode is formed, and a second surface, which is opposite the first surface;
the second semiconductor element includes a third surface, on which the second electrode is formed, and a fourth surface, which is opposite the third surface; and
the first semiconductor element and the second semiconductor element are stacked such that the second surface faces the third surface.

Claim 9 (Canceled).

Claim 10 (Original): A semiconductor package according to claim 8, wherein the fourth surface is substantially devoid of the resin material, and the resin material is applied to substantially the remainder of the package.

Claim 11 (Canceled).

Claim 12 (Original): A semiconductor package according to claim 2, wherein each of the second semiconductor element and the first semiconductor element has two sets of substantially parallel edges, and each of the longer and the shorter leads extends substantially orthogonally to each edge.

Claim 13 (Canceled).

Claim 14 (Original): A semiconductor package according to claim 2, wherein the longer lead and the shorter lead extend outwardly in substantially the same plane.

Claim 15 (Canceled).

Claim 16 (Original): A semiconductor package according to claim 8, wherein the second surface is adhered to the third surface.

Claim 17-32 (Canceled)

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Claim 33 (Currently amended): A semiconductor package, comprising:
a tape carrier having a longitudinal extension and two side edges running parallel to the longitudinal extension;
a first semiconductor element mounted on the tape carrier between the two side edges;
a second semiconductor element mounted on the tape carrier between the two side edges;
a short lead provided on the tape carrier, and being connected to the first semiconductor element; and
a long lead provided on the tape carrier, and being connected to the second semiconductor element.

Claim 34 (Previously presented): A semiconductor package recited in claim 33, wherein the second semiconductor element is disposed on the first semiconductor element.

Claim 35 (Currently amended): ~~A semiconductor package recited in claim 34;~~
A semiconductor package, comprising:
a tape carrier;
a first semiconductor element mounted on the tape carrier;
a second semiconductor element mounted on the tape carrier;
a short lead provided on the tape carrier, and being connected to the first semiconductor element; and
a long lead provided on the tape carrier, and being connected to the second semiconductor element;
wherein the second semiconductor element is disposed on the first semiconductor element;

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wherein the first semiconductor element has a surface and a first electrode, on which surface the first electrode is provided;

wherein the long lead has two ends and a first land, the one end being connected to the first electrode and the other end forming the first land on the tape carrier;

wherein the second semiconductor element has a surface and a second electrode, on which surface the second electrode is provided, and the first semiconductor element is stacked; and

wherein the short lead has two ends and a second land, the one end being connected to the second electrode and the other end forming a second land on the tape carrier;

and wherein the semiconductor package further comprises a resin material which seals the first semiconductor element, the second semiconductor element, the longer lead and the shorter lead; and

solder balls, which are mounted on the first and second lands for external connection

Claim 36 (Previously presented): A semiconductor package according to claim 35, further comprising at least another longer lead and at least another shorter lead, wherein each of the longer leads and each of the shorter leads are arranged so as to alternate with each other.

Claim 37 (Previously presented): A semiconductor package according to claim 35, wherein the second semiconductor element is larger than the first semiconductor element, and comprises a surface area that faces the first semiconductor element and the second electrode is disposed outside said area.

Claim 38 (Previously presented): A semiconductor package according to claim 35, wherein:

the first semiconductor element includes a first surface, on which the first electrode is formed, and a second surface, which is opposite the first surface;

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the second semiconductor element includes a third surface, on which the second electrode is formed, and a fourth surface, which is opposite the third surface; and

the first semiconductor element and the second semiconductor element are stacked such that the second surface faces the third surface.

Claim 39 (Previously presented): A semiconductor package according to claim 38, wherein the fourth surface is substantially devoid of the resin material, and the resin material is applied to substantially the remainder of the package.

Claim 40 (Previously presented): A semiconductor package according to claim 35, wherein each of the second semiconductor element and the first semiconductor element has two sets of substantially parallel edges, and each of the longer and the shorter leads extends substantially orthogonally to each edge.

Claim 41 (Previously presented): A semiconductor package according to claim 35, wherein the longer lead and the shorter lead extend outwardly in substantially the same plane.

Claim 42 (Previously presented): A semiconductor package according to claim 38, wherein the second surface is adhered to the third surface.

Claim 43 (Withdrawn): A semiconductor package according to claim 34, wherein:
the first semiconductor element has an upper surface and a first electrode, on which upper surface the first electrode is provided;

the short lead is connected to the first electrode;

the second semiconductor element has an upper surface and a second electrode, on which upper surface the second electrode is provided; and

the long lead is connected to the second electrode;

said semiconductor package further comprising:

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a third semiconductor element having an upper surface and a third electrode, on which upper surface the third electrode is provided;

a further lead, which is shorter than the short lead, provided on the tape carrier and being connected to the third electrode; and

a molding member, which seals the first semiconductor element, the second semiconductor element, the third semiconductor element, the first lead, the second lead and the third lead.

Claim 44 (Withdrawn): A semiconductor package according to claim 34, wherein the first semiconductor element has an upper surface and a first electrode, on which upper surface the first electrode is provided;

wherein the short lead is connected to the first electrode; and

wherein the second semiconductor element has an upper surface and a second electrode, on which upper surface the second electrode is provided;

the semiconductor package further comprising a third semiconductor element having an upper surface and a third electrode, on which upper surface the third electrode is provided, the third semiconductor element being disposed such that side surfaces of the first semiconductor element and the third semiconductor element are opposite each other and a space is formed therebetween;

a further short lead provided on the tape carrier and being connected to the third electrode; and

a molding member which seals the first semiconductor element, the second semiconductor element, the third semiconductor element, the long lead and the short leads, wherein

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the lower surface of the second semiconductor element is adhered to both the upper surface of the first semiconductor element and the upper surface of the third semiconductor element.

Claim 45 (Previously presented): ~~A semiconductor package according to claim 34,~~

A semiconductor package, comprising:

a tape carrier;

a first semiconductor element mounted on the tape carrier;

a second semiconductor element mounted on the tape carrier;

a short lead provided on the tape carrier, and being connected to the first semiconductor element; and

a long lead provided on the tape carrier, and being connected to the second semiconductor element;

wherein the second semiconductor element is disposed on the first semiconductor element;

wherein the tape carrier has a device hole, and lands which are arranged in a grid pattern;

wherein each lead has an outer lead portion and an inner lead portion, which outer lead portions are connected to the plurality of lands;

wherein a solder resist is provided on the lead which includes an opening through which the land is exposed;

wherein a metal ball is connected to the land via the opening; and

wherein the inner lead portions, which extend from a periphery of the device hole toward a center of the device hole, have several different lengths.

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Claim 46 (Previously presented): A semiconductor package according to claim 45, wherein the inner lead portions having different lengths are disposed regularly.

Claim 47 (Previously presented): ~~A semiconductor package as recited in claim 34,~~

A semiconductor package, comprising:

a tape carrier;

a first semiconductor element mounted on the tape carrier;

a second semiconductor element mounted on the tape carrier;

a short lead provided on the tape carrier, and being connected to the first semiconductor element; and

a long lead provided on the tape carrier, and being connected to the second semiconductor element;

wherein the second semiconductor element is disposed on the first semiconductor element;

wherein the tape carrier has a device hole formed therein, a lower surface, and lands arranged in a grid pattern;

wherein openings are formed through which the lands are exposed to the lower surface side of the base tape;

wherein the leads have outer lead portions and inner lead portions, the outer lead portions being connected to the plurality of lands;

wherein a solder resist is provided on the leads;

wherein a metal ball is connected to the land via the opening; and

wherein the inner lead portions of the leads extend from a periphery of the device hole toward a center of the device hole and have several different lengths.

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Claim 48 (Previously presented): A semiconductor package according to claim 47, wherein the solder resist includes openings through which the upper surfaces of the lands are exposed.

Claim 49 (Previously presented): A semiconductor package according to claim 47, wherein the inner lead portions are in sets of different lengths and are disposed at substantially regular intervals.

Claim 50 (Previously presented): A semiconductor package according to claim 34, wherein the first semiconductor element has upper and lower surfaces and a first electrode, on which upper surface the first electrode is provided;

wherein the short lead is connected to the first electrode;

wherein the second semiconductor element has upper and lower surfaces and a second electrode, on which upper surface the second electrode is provided; and

wherein the long lead is connected to the second electrode;

the semiconductor package further comprising a third semiconductor element having an upper surface and a third electrode, on which upper surface the third electrode is provided, the second semiconductor element being disposed such that side surfaces of the second semiconductor element and the third semiconductor element are opposite each other, with a space formed therebetween, the second semiconductor element and the third semiconductor element being adhered to the upper surface of the first semiconductor element;

a further long lead which is connected to the third electrode; and

a molding member which seals the first semiconductor element, the second semiconductor element, the third semiconductor element, and the long leads and the short lead.

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Claim 51 (Previously presented): A semiconductor package recited in claim 33, wherein the tape carrier is sandwiched between the second semiconductor element and the first semiconductor element.

Claim 52 (Previously presented): A semiconductor package recited in claim 51, wherein the first semiconductor element has a lower surface, on which lower surface a first electrode is provided;

wherein the short lead is connected to the first electrode;

wherein the second semiconductor element has an upper surface, on which upper surface a second electrode is provided;

wherein the long lead is connected to the second electrode;

wherein a molding member seals the first semiconductor element, the second semiconductor element, and the long lead and the short lead; and

wherein the first semiconductor element is held so as to be spaced apart from the second semiconductor element.

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